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|------------------------|-----------------|
| Application Number | 09/527,634 |
| Filing Date | March 17, 2000 |
| First Named Inventor | Lo, Sun Man |
| Group Art Unit | 2812 |
| Examiner Name | Eron J. Sorrell |
| Attorney Docket Number | 010262-013100US |

Total Number of Pages in This Submission 10

ENCLOSURES (check all that apply)☐ Fee Transmittal Form☐ Fee Attached☒ Amendment / Reply☐ After Final☐ Affidavits/declaration(s)☐ Extension of Time Request☐ Express Abandonment Request☐ Information Disclosure Statement☐ Certified Copy of Priority Document(s)☐ Response to Missing Parts/
Incomplete Application☐ Response to Missing Parts
under 37 CFR 1.52 or 1.53☐ Assignment Papers
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Townsend and Townsend and Crew LLP

Paul C. Haughey

Reg. No. 31,836

Signature

Date

December 13, 2002

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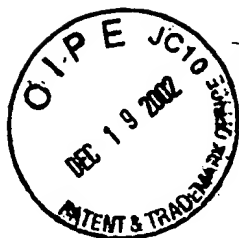
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Attorney Docket No.: 010262-013100US

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

GLENN WEGNER ET AL.

Application No.: 09/527,634

Filed: March 17, 2000

For: UART AUTOMATIC HALF-DUPLEX DIRECTION CONTROL WITH PROGRAMMABLE DELAY

Examiner: Eron J. Sorrell

Art Unit: 2812

AMENDMENT

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Assistant Commissioner for Patents
Washington, D.C. 20231

December 13, 2002

Sir:

In response to the Office Action mailed September 13, 2002, please amend the above-identified application as follows:

IN THE SPECIFICATION:

On page 3, please replace the paragraph beginning at line 7 with the following paragraph:

A1
--Fig. 1 is a block diagram of a UART 10. The UART includes eight channels 12. Channel 0 indicates the internal circuitry for that channel, which is not shown but would be the same for the other eight channels. In particular, it has a 64-bit transmit first in/first out (FIFO) buffer 14 and a 64-byte receive FIFO 16. The channel also includes other control circuitry and registers. The channels interface via I/O lines 18 to serial data communication lines. The data can be provided through an internal bus 20 to an internal FIFO manager 22. The FIFO manager provides the data in both directions through a second internal bus 24 to a PCI local bus interface 26. This interfaces with a PCI bus 28. Fig. 1 also shows PCI bus configuration registers 13, an EEPROM interface